

LA2230, 2230M

RDS Decoder

Overview

The LA2230 and LA2230M are RDS demodulator ICs with an on-chip 57kHz bandpass filter and ARI-SK and DK signal identifiers. A high-performance, cost-effective RDS decoder system with group/block synchronization and error detection/correction can be built using an LC7070 series device with the LA2230 or LA2230M.

LA2230 and LA2230M feature adjustable ARI detection sensitivity for improved interference rejection and a high-speed charging circuit for rapid power-on start-up. Including the 57kHz bandpass filter on-chip results in lower-cost designs that use less PCB area.

The LA2230 and LA2230M operate from a 5V supply and are avilable in 24-pin DIPs and 24-pin MFPs, respectively.

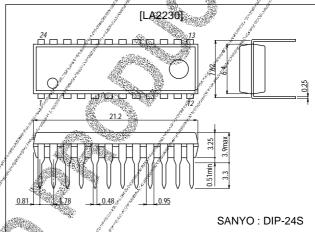
Features

- 57kHz bandpass filter.
- Adjustable ARI detection sensitivity.
- High-speed charging circuit.
- ARI and RDS signal demodulation.
- Bit-rate clock recovery.
- RDS, DK and SK identification outputs.
- 5V supply.
- 24-pin DIP (LA2230) and 24-pin MFP (LA2230M)

Package Dimensions

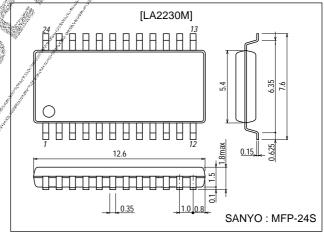
unit:mr

3067-DIP24S



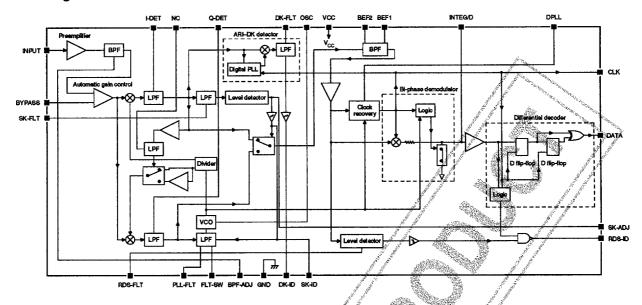
unit:mm

3112-MFP24S



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Block Diagram



Pin Description

Number	Name	Description				
1	DK-FLT	DK in-phase detector lowpass filter connection.				
2	Q-DET	Quadrature detection output				
3	NC	No connection Should be left open				
4	I-DET	In-phase detector output				
5	BYPASS	Bandpass filter bypass capacitor connection				
6	INPUT	ARI and RDS signal input				
7	SK-FLT	SK lowpass filter capacitor connection				
8	RDS-FLT	RDS lowpass filter capacitor connection				
9	PLL-FLT profession	PLL loop filter connection				
10	FLT-SW	PLL toop fifter switch				
11	BPF-ADÜ 🚧	Bandpass filter adjustment variable resistor connection				
12	GND, (Ground				
13	DK-ID **	ARI-DK signal identification output				
14	∫ \$K-ID 🦓 🦓	ARI-SK signal identification output				
15	RDS-ID	RDS signal dentification output				
16	🥕 / SK-ADJ 😘	ARI detection sensitivity adjustment variable resistor connection				
17	DATA	Data gutput				
18	CLK	Bit-fațe clock output				
19	(DPLL //	Digital PLL lowpass filter connection				
20	INTEG/D /	Integrator and dump capacitor connection				
21	B £ F1 //	Dand elimination filter connections				
22	BEF2	and-elimination filter connections				
23	V _{CC} /	5V supply				
24	O\$C/	Ceramic resonator connection				

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max	13, 14, 15, and 23 pin		V
		LA2230 : Ta≤80°C	450	
Power dissipation	Pd max	LA2230M : Ta≤37.5°C	450	mW
		LA2230M : Ta=80°C	280	
Operating temperature range	Topr	A STATE OF THE STA	-30° to, +80.	°C
Storage temperature range	Tstg		-40 to +125 (LA2230) -40 to +150 (LA2230M)	c

Recommended Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol		Conditions		Ratings	Unit
Supply voltage	Vcc	23 pin			5	V
Supply voltage range	V _{CC} op	23 pin	11	, 130/15 . N. 100/2	🦨 🔏 4.7 to 5.5	V

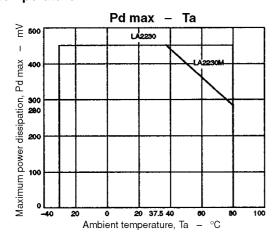
Electrical Characteristics at Ta = 25°C, $V_{CC}=5V$

Parameter	Symbol	Çönditions	200	Ratings		Unit	
Falametei		Conditions	miń	typ	max	Offic	
Quiescent supply current	Icco		14	22	28	mA	
RDS detection sensitivity	V _{I1}	V _{INPUT} =minimum signal for HIGH to Low transition on RDS-ID	*	0.4	1.0	mV	
SK detection sensitivity	V _{I2}	V _{INPUT} =minimum signal for HIGH to-Low transition on SK-ID		1.0	2.0	mV	
DK detection sensitivity	V _{I3}	VINPUT=minimum signal for HIGH-to-Low transition on SK-ID		1.1	2.0	mV	
RDS detection maximum input signal	V _{I4}	V _{INPUT} =maximum (ARI + RDS) signal for HIGH-to- Low transition on RDS-ID	30	50		mV	
NDS detection maximum input signal	V _{I5}	VINPUT=maximum RDS signal for RDS data correctly demodulated	250			mV	
DK detection maximum input signal	V ₁₆ ,	VINPUT maximum ARI signal for HIGH-to-Low transition on DK-ID	75	100		mV	
CLK and DATA LOW-level output voltage	V _{OL}		0	0.1	0.3	V	
CLK and DATA HIGH-level output voltage	[,] V∕OH		4.7	4.9	5.0	V	
Bandpass filter voltage gain	/ /V _G	f=57KHz	9.0	12.5	17.0	dB	
gg		f=60kHz. See note 1	0	2.5	6.0	dB	
Bandpass filter attenuation	α	1=54kHz. See note 1.	0	3.5	6.0	dB	
		f≟38kHz. See nøte 1.	33	39		dB	
PLL capture range	CP.	Low side, √INPUT=5mV sine wave		-0.9		- %	
T LE capture range		High side, VINPUT=5mV sine wave		1.5		70	
Bit-rate clock jitter	t _j	, de state de la companya del companya de la companya del companya de la companya	±8	±9	±10	μs	
RDS lock-up time	^I RDS	Peniod from V _{INPUT} =3mV RDS signal to HIGH-toLOW transition on RDS-ID		35		ms	
SK lock-up time	[†] tsk /	Period from V _{INPUT} =8mV ARI signal to HIGH- நீட்OW transition on SK-ID		45		ms	
SK + RDS lock-up time	tsk + ^R D\$	Period from V _{INPUT} =8.5mV (ARI + RDS) signal to HIGH-toLOW transition on RDS-ID		80	·	ms	
VCO free-running frequency	fyco		453	456	459	kHz	
BPF adjustment resistance	RADJ	V _{INPUT} =100mV at 57kHz. See note 2.	5.6	8.0	10.6	kΩ	

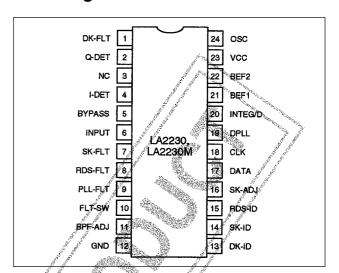
- Notes
 1. 0dB is referenced to the filter output with f=57kHz.
- 2. Resistance between BPF-ADJ and GND when $V_{\mbox{\footnotesize{BYPASS}}}$ is at its maximum.

Typical Performance Characteristics

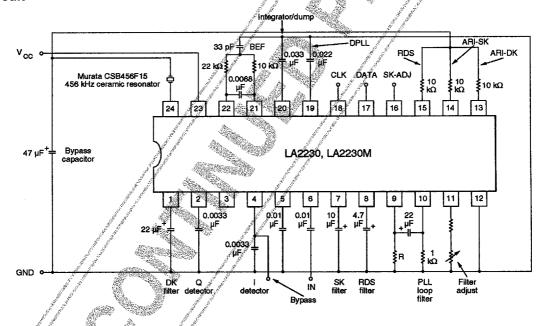
Maximum power dissipation vs. ambient temperature



Pin Assignment



Test Circuit



Notes

 $R=1.2M\Omega$ for the LA2230, and 1.5M Ω for the LA2230M.

Operating Information

57kHz Bandpass Filter Adjustment

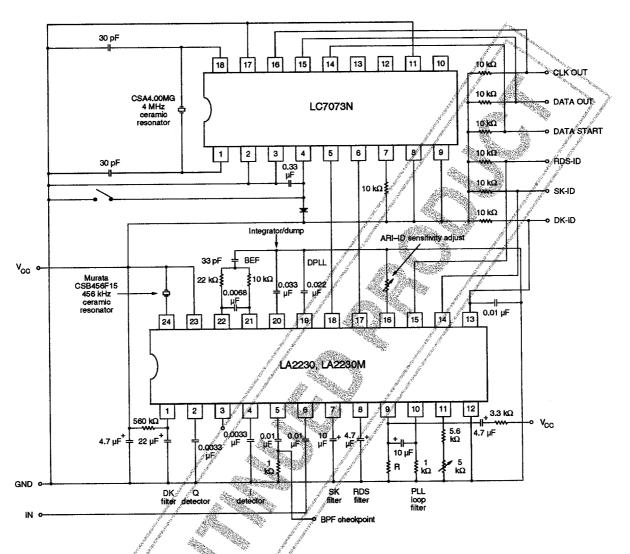
- 1. Adjust the variable resistor connected to BPF-ADJ to obtain the maximum signal level measured at I-DET or BEF2.
- 2. When $V_{INPUT}=1 \text{mV}$ RDS signal, check I-DET or BEF2 for a bi-phase output signal as shown in the following figure. Note that the ALC circuit will not operate when $V_{INPUT} \leq 1 \text{mV}$.



3. Check the BPF checkpoint signal level when V_{INPUT}=3 to 6mV or greater RDS signal.

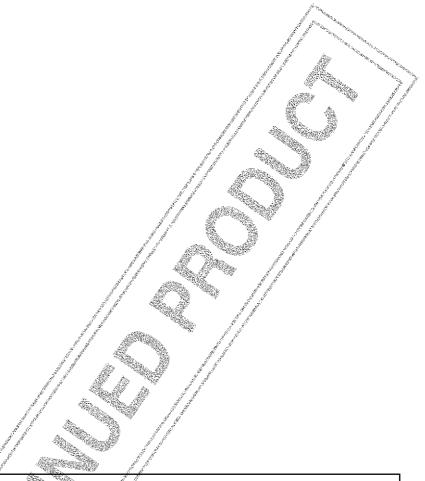
Typical Application

The recommended input is a 3 to 6mV RDS signal with $\Delta f = \pm 2kHz$.



Notes

 $R=1.2M\Omega$ for the LA2230, and 1.5MQ for the LA2230M.



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