

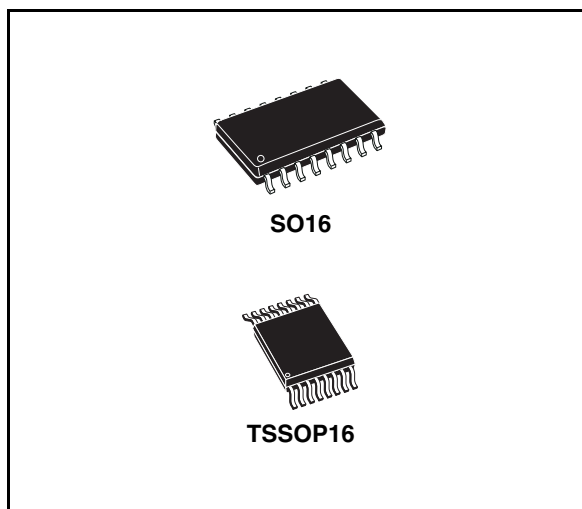
## Single chip RDS demodulator + filter

### Features

- Very high RDS demodulation quality with improved digital signal processing
- High performance, 57 kHz bandpass filter (8<sup>th</sup> order)
- Filter adjustment free and without external components
- Purely digital RDS Demodulation without external components
- ARI (SK indication) and RDS signal quality output
- 4.332 MHz crystal oscillator (8.664 and 17.328 MHz optional)
- Low noise CMOS technology
- Low radiation

### Description

The TDA7479 recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations and operates in accordance with the EBU (European Broadcasting Union) specifications.



The device is made up of two sections: a cascaded antialiasing + switched capacitors 8<sup>th</sup> bandpass filter for precise RDS band selection and a demodulating section that performs the extraction of RDS data stream (RDDA) and clock (RDCL), to be further processed by a suitable RDS decoder.

Outputs for RDS signal quality and ARI indication are also present.

**Table 1. Device summary**

Order code	Package	Packing
E-TDA7479D <sup>(1)</sup>	SO16	Tube
E-TDA7479AD <sup>(1)</sup>	TSSOP16	Tube

1. Device in ECOPACK® package (see [Section 5: Package information on page 9](#)).

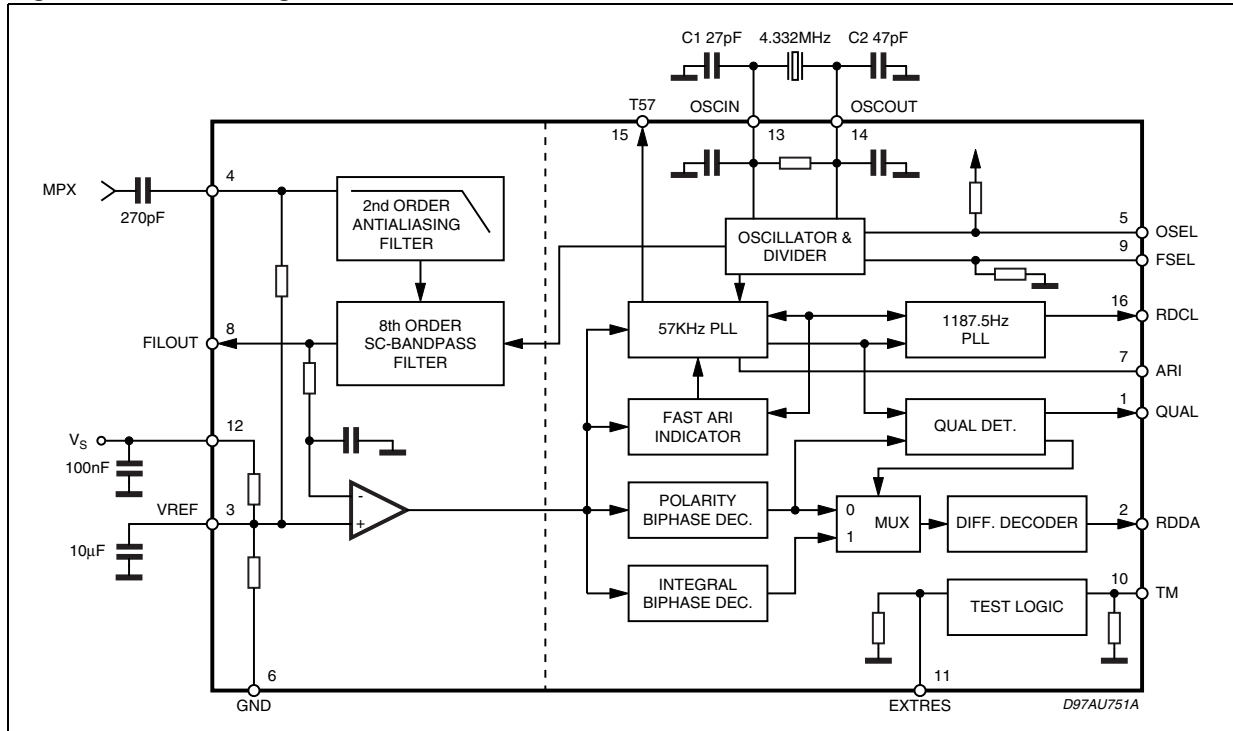
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# 1 Block diagram and pin description

## 1.1 Block diagram

Figure 1. Block diagram



## 1.2 Pin description

Figure 2. Pin connection (top view)

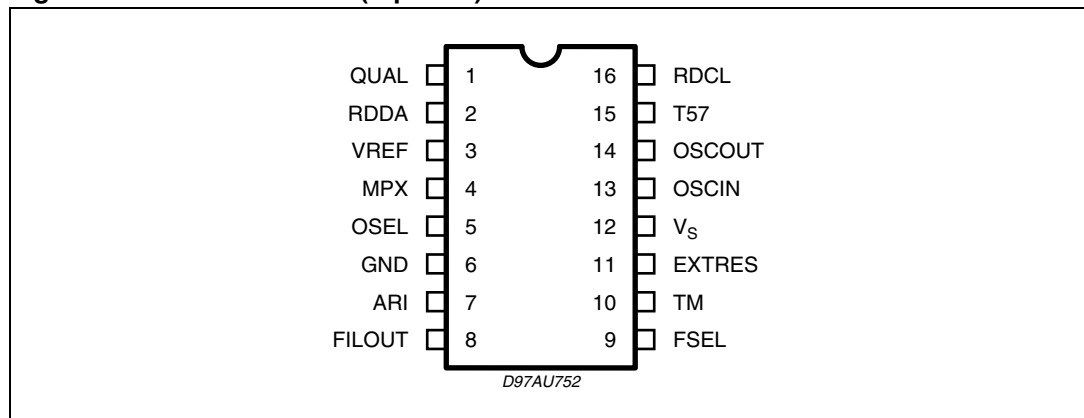


Table 2. Pin description

No pin	Name	Description
1	QUAL	Output for signal quality indication (High = good)
2	RDDA	RDS data output
3	VREF	Reference voltage
4	MPX	RDS input signal
5	OSEL	Oscillator selector pin: – open, closed to $V_S$ = quartz oscillator – closed to GND = external driven
6	GND	Ground
7	ARI	Output for ARI indication: – high when RDS+ARI are present – high when only ARI is present – low when only RDS is present – undefined when nos signal is present
8	FILOUT	Filter output
9	FSEL	Frequency selector pin: – 100 kHz to $V_S$ = 17.328 MHz – open = 4.332MHz – closed to VS = 8.664 MHz
10	TM	Test mode pin: – open = normal operation – closed to VS = test mode
11	EXTRES	Reset pin: – open = run mode – -closed to VS = reset condition
12	$V_S$	Supply voltage
13	OSCIN	Oscillator input
14	OSCOUT	Oscillator output
15	T57	Testing output pin: 57 kHz clock output
16	RDCL	RDS clock output 1187.5 Hz

## 2 Electrical specification

### 2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter		SO16	TSSOP16	Unit
$R_{th\ j-case}$	Thermal resistance junction to case	Max.	200	160	°C/W

### 2.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_S$	Supply voltage	-0.3 to 7	V
$T_{op}$	Operating temperature range	-40 to 85	°C
$T_{stg}$	Storage temperature	-55 to 150	°C

### 2.3 Electrical characteristics

Table 5. Electrical characteristics

( $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 5\text{V}$ , unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage		4.5	5	5.5	V
$I_S$	Supply current			7.5	11.0	mA
<b>Filter</b>						
$f_C$	Center frequency		56.5	57	57.5	kHz
BW	3dB Bandwidth		2.5	3	3.5	kHz
G	Gain	$f = 57\text{ kHz}$	18	20	22	dB
A	Attenuation	$\Delta f \pm 4\text{ kHz}$	18	22		dB
		$f = 38\text{ kHz}$	50	60		dB
		$f = 67\text{ kHz}$	35	45		dB
$R_I$	Input impedance of MPX		80	120	150	$\text{K}\Omega$
$R_L$	Load impedance on FILOUT		1			$\text{M}\Omega$
S/N	Signal to noise ratio	$V_{IN} = 3\text{ mVrms}$	30	40		dB
$V_{IN}$	MPX input signal	$f = 19\text{ kHz}$ ; $T_3 \leq 40\text{ dB}^{(1)}$ $f = 57\text{ kHz}$ (RDS+ ARI)			1000 50	$\text{mV}_{\text{RMS}}$ $\text{mV}_{\text{RMS}}$
$S_{\text{RDS}}$	RDS detection sensitivity		1			$\text{mVrms}$
$S_{\text{ARI}}$	ARI Detection Sensitivity		3			$\text{mVrms}$

**Table 5. Electrical characteristics (continued)**  
 ( $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 5\text{V}$ , unless otherwise specified)

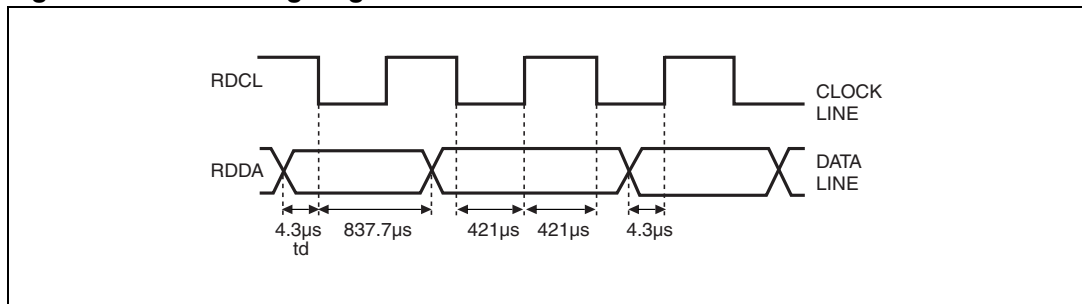
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{REF}$	Reference			$V_S/2$		V
<b>Demodulator</b>						
<i>Input pins (EXTRES, FSEL, TM:) all with internal pull down resistor</i>						
<i>Input pin (OSEL): with internal pull up resistor</i>						
$I_{PD}$	Input current	$V_{IN} = 5\text{ V}$ (pull-down input)	15		30	$\mu\text{A}$
$I_{PU}$	Input current	$V_{IN} = 0\text{ V}$ (pull-up input)	-25		-10	$\mu\text{A}$
$V_{IH}$	Input voltage high		$0.7 \cdot V_S$	$0.8 \cdot V_S$		V
$V_{IL}$	Input voltage low			$0.2 \cdot V_S$	$0.3 \cdot V_S$	V
<i>Output pins (RDCL, RDDA, ARI, QUAL, T57)</i>						
$V_{OH}$	Output voltage high	$I_L = 0.5\text{mA}$	4	4.6		V
$V_{OL}$	Output voltage low	$I_L = 0.5\text{mA}$		0.4	1	V
<b>Oscillator</b>						
$V_{CLL}$	Input level OSCIN pin	OSEL = open circuit			1	V
$V_{CLH}$	Input level OSCIN pin	OSEL = open circuit	4			V
	Amplitude OSCOUT	OSEL = open circuit		4.5		V
$V_{PP}$	Amplitude OSCIN (for external drive)	OSEL = GND, $f = 4.332\text{ MHz}$		100		mVpp
		OSEL = GND, $f = 8.664\text{ MHz}$		120		mVpp
		OSEL = GND, $f = 17.328\text{ MHz}$		150		mVpp

1. The 3<sup>rd</sup> harmonic (57 kHz) must be less than -40 dB with respect to the input signal plus gain.

### 3 Output timing

The RDS (1187.5Hz) output clock on RDCL line is synchronized to the incoming data. According to the internal PLL lock condition data change can result on the falling or on the rising clock edge (see [Figure 3](#)). Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7  $\mu$ s after the clock transition.

**Figure 3. RDS timing diagram**



## 4 Oscillator controls (FSEL, OSEL)

Three different crystal frequencies can be used. The adoption of the internal clock divider to the external crystal is achieved via the input pin FSEL. See the following table for reference:

**Table 6. Crystal frequencies**

Crystal	FSEL (pin configuration)
4.332MHz 8.664MHz 17.328MHz	connected to GND or open connected to Vs external resistor of 100K to Vs

A special mode is introduced to reduce EMI. With pin OSEL connected to GND the internal oscillator is switched off and an external sinusoidal frequency could be applied on OSCIN. The peak to peak voltage of this signal can be reduced down to 60mV.

In this mode the frequency selection via FSEL is still active.

Suggested values of C1 and C2 are shown in the following table:

**Table 7. C1 and C2 value**

Crystal	C1	C2
4.332MHz	27pF	47pF
8.664MHz	27pF	-
17.328MHz	27pF	-



## 5 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK<sup>®</sup> packages. ECOPACK<sup>®</sup> packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

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**Figure 4. SO16 mechanical data and package dimensions**

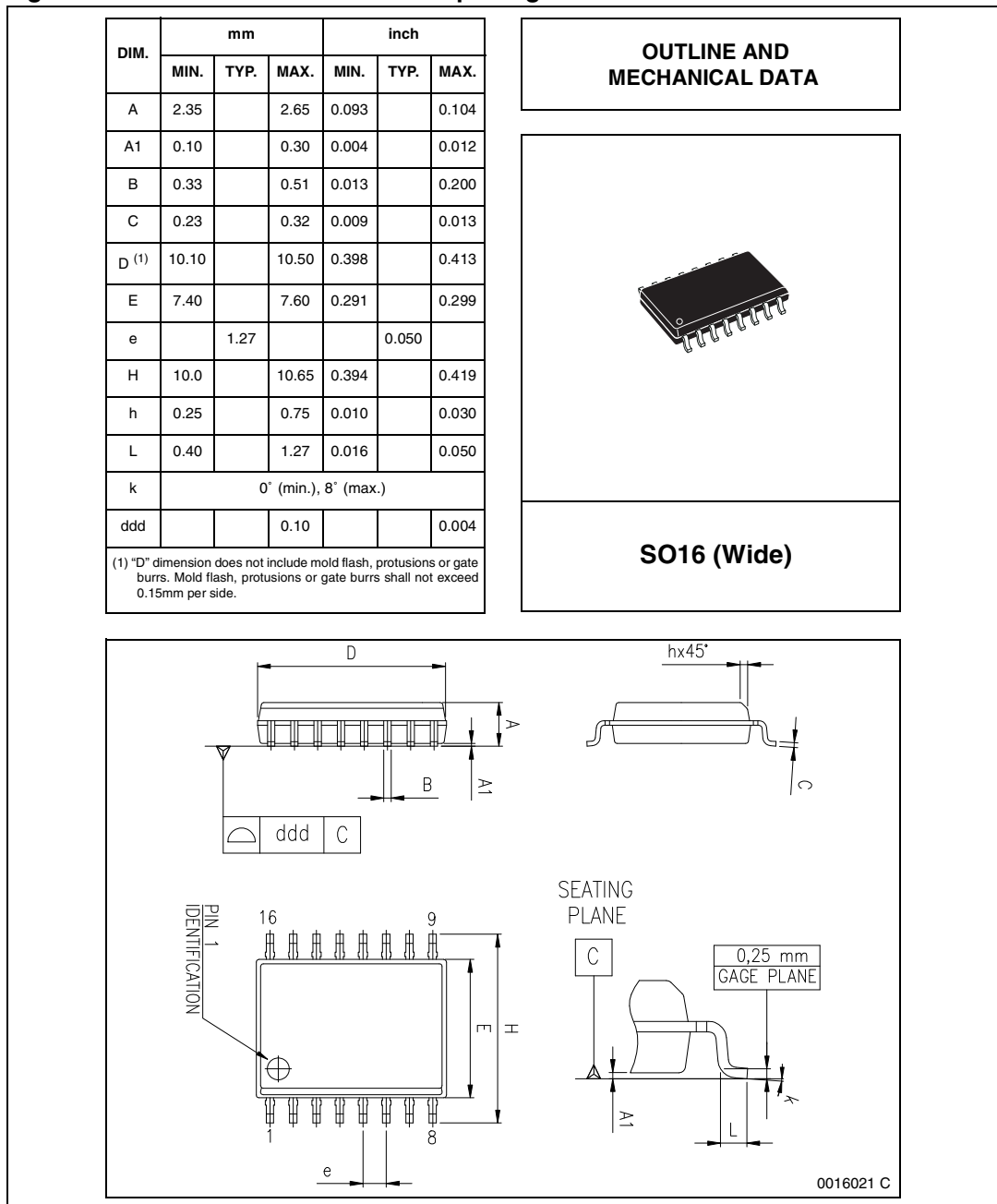
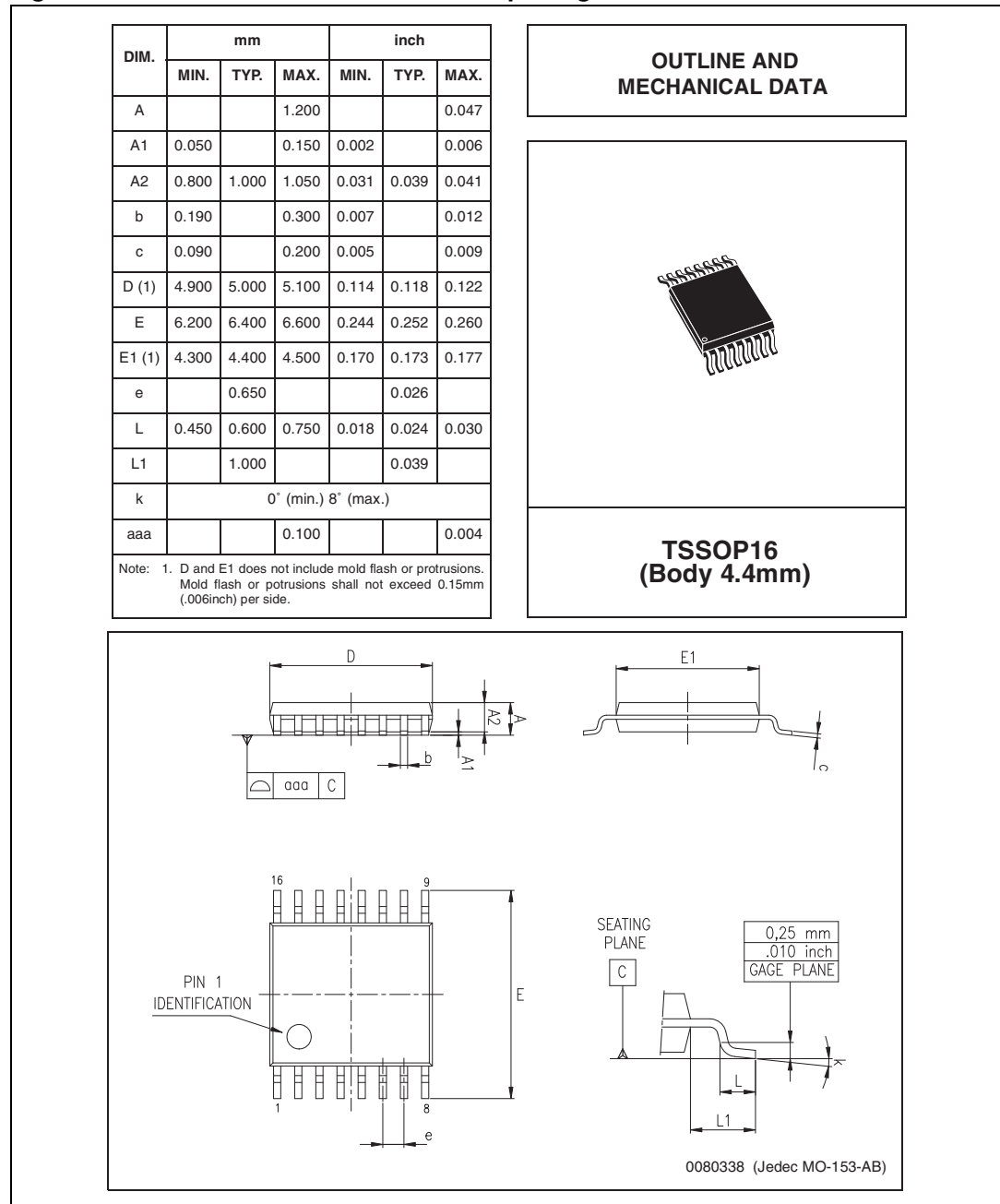


Figure 5. TSSOP16 mechanical data and package dimensions



## 6 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
10-Sep-2004	4	Initial release.
20-Nov-2004	5	Add in <a href="#">Table 5: Electrical characteristics on page 5</a> the “RDS and ARI Detection Sensitivity” parameters.
02-Dec-2004	6	Modified the order codes table.
04-Nov-2008	7	Document reformatted. Updated <a href="#">Table 1: Device summary on page 1</a> . Updated <a href="#">Section 5: Package information on page 9</a> .
16-Sept-2013	8	Updated Disclaimer

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